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EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 03/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/802,289	SAULSBURY ET AL.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/11/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 18-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 8-16, and 18-21* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 2, and 10-16, and 18-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 2, lines 1-2, "every two of said N-number of processing paths" is meaningless in the situation when N=1 since N number was not specifically defined.

In claim 10, lines 9-10, the statement: "an integer processing unit and a floating point processing unit within said one or more processing pipeline" is unclear because based on lines 3-6 in the claim, the execute unit in the pipeline may comprise only an integer processing unit, a floating point processing unit **or** a load/store processing unit.

In claim 11, lines 9-10, the statement: "an I/O link configured to communicate with other of said one or more

processor chips" is unclear because based on line 3, in the claim, there may be only one processor chip in the system since "one or more processor chips" was mentioned.

In claim 12, line 2, "every two of said N-number of processing paths" is meaningless in the situation when N=1.

Applicant is required to review the claims and correct all language which does not comply with 35 U.S.C. § 112, second paragraph.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 5, 6, 8-13, 15, 16, and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masubuchi (USP

5,530,817), hereafter referred to as Masubuchi'817 in view of Cook (USP 5,301,340), hereafter referred to as Cook'340.

Referring to claim 1, Masubuchi'817 discloses, as claimed, a processing core (processing elements: 100, and 200 see Fig. 1) comprising: one or more processing pipelines having a total of N-number of processing paths (N=2 for the Masubuchi'817's system shown in Fig. 1), each of said processing paths for processing instructions on M-bit data words (the data can be either 16, 32 or 64 bits); and a plurality of register files (12 and 22, see Fig. 1), each having Q-number of registers (note Masubuchi'817's register files (12 and 22 see Fig. 1) inherently comprises Q register each), said Q-number of registers being M-bits wide; wherein said Q-number of registers within each of said plurality of register files (12 and 22 see Fig. 1) are both private and global registers (since they can be used as both private and global registers), wherein when a value (the data value exchanged between the register files 12 and 22 see Fig. 1) is written to one of said Q-number of said registers which is a private register (since the data value are only exchanged between the register files 12 and 22 see Figs. 3 and 4) within one of said plurality of register files (the register files 12 and 22 see Fig. 1), said value is not propagated to a

corresponding register in the other of said plurality of register files.

Referring to claim 10, Masubuchi'817 discloses, as best understood, as claimed a VLIW processing core (processing sections: 100, and 200 see Fig. 1) comprising: one or more processing pipelines (such as pipeline in 100, and pipeline in 200, see Fig. 1) each including a fetch stage (inherent stage in a pipeline), a decode stage (inherent stage in a pipeline), an execute stage (inherent stage in a pipeline), and a write-back stage (inherent stage in a pipeline), said execute stage having an execute unit comprising an integer processing unit (such as ALU1 13 and ALU2 14 in for the data operation inside 100, see Fig. 1), a load/store processing unit (such as ALU 23 in for the LDA operation inside 200, see Fig. 1), a floating point processing unit or any combination of one or more of said integer processing units, said load/store processing units, and said floating point processing units; and a register file (12 or 22 see Fig. 1) for each of said one or more processing pipelines (note as shown in Fig. 1, each pipeline has one register file 12 or 22 see Fig. 1); wherein an integer processing unit and a floating point processing unit within said one or more processing pipelines both access said register file (12 or 22 see Fig. 1), the register file is comprised of Q-number of

registers (12 or 22 see Fig. 1), said Q-number of registers (12 or 22 see Fig. 1) comprise both private and global registers (since they can be used as both private and global registers), when a value (the data value exchanged between the register files 12 and 22 see Fig. 1) is written to one of said Q-number of said registers which is a private register (since the data value are only exchanged between the register files 12 and 22 see Fig. 1) within one of said plurality of register files (12 or 22 see Fig. 1), said value is not propagated to a corresponding register in another register file within VLIW processing core (comprising processing sections: 100, and 200 see Fig. 1). Note Masubuchi'817 also discloses the limitations of claims 5, 15, 6, and 16 as set forth above in claim 10 wherein N-number (N=2 for the Masubuchi'817's system shown in Fig. 1), and M-bit data words (the data can be either 16, 32 or 64 bits) are set forth above.

Referring to claim 11, Masubuchi'817 discloses, as best understood, as claimed in a computer system, a scalable computer processing architecture, comprising: one or more processor chips (see Fig. 1, and col. 3, lines 22-23, regarding using a plurality of chips. Further, as set forth in the 112, 2nd paragraph rejection, "one or more processor chips" can be interpreted as having only one processor chip in the system),

each comprising: a processing core (processing sections: 100, and 200 see Fig. 1), including: a processing pipeline having N-number (N=2 in Fig. 1) of processing paths, each of said processing paths for processing instructions on M-bit data word (the data can be either 16, 32 or 64 bits); and one or more register (12 or 22 see Fig. 1), each having Q-number of registers (note Q is a variant. Masubuchi'817's VLIW is certainly having Q number), said Q-number of registers being M-bits wide; an I/O link (certainly exist when using a plurality of chips) configured to communicate with other of said one or more processor chips or with I/O devices; a communication controller (the control unit inside the CPU of Masubuchi'817's system is broadly interpreted as a communication controller) in electrical communication with said processing core and said I/O link (certainly exist when using a plurality of chips); said communication controller for controlling the exchange of data between a first one of said one or more processor chips and said other of said one or more processor chips (note as set forth in the 112, 2nd paragraph rejection, there may be only one processor chip in the system since "one or more processor chips" was mentioned in the claim. Therefore, the limitation is questionable); wherein said computer processing architecture can be scaled larger by connecting together two or more of said

processor chips (see col. 3, lines 22-23, regarding using a plurality of chips) in parallel via said I/O links link (as set forth, certainly exist when using a plurality of chips) of said processor chips, so as to create multiple processing core (the core comprising processing sections: 100, and 200 see Fig. 1) pipelines which share data therebetween, said Q-number of registers within each of said plurality of register (12 or 22 see Fig. 1) are either private or global registers (since they can be used as both private and global registers), wherein when a value (the data value exchanged between the register files 12 and 22 see Fig. 1) is written to one of said Q-number of said registers which is a private register (since the data value are only exchanged between the register files 12 and 22 see Fig. 1) within one of said plurality of register files register (12 or 22 see Fig. 1), said value is not propagated to a corresponding register in the other of said plurality of register files.

Masubuchi'817 discloses the claimed invention except for: the feature that when a value is written to one of said Q-number of said registers which is a global register within one of said plurality of register files, said value is propagated to a corresponding global register in the other of said plurality of register files (in claims 1, 10, and 11); each of said plurality of register files is connected to a bus, and a value written to

a global register in one of said plurality of register files is propagated to a corresponding global register in the other of said plurality of register files across said bus (in claims 8, and 19); and said plurality of register files are connected together in serial, and a value written to a first global register in a first of said plurality of register files is propagated to a corresponding first global in a second of said plurality of register files connected directly to said first of said plurality of register files (in claims 9 and 20).

Cook'340 discloses a system comprising the feature that when a value is written to one of said Q-number of said registers (RFs inside chips 51-54, see Fig. 5) which is a global register within one of said plurality of register files, said value is propagated (see Col. 4, lines 42-47, regarding the data written by any ALUs is "broadcast" via bus 55 to all registers) to a corresponding global register (see Fig. 5) in the other of said plurality of register files (RFs inside chips 51-54, see Fig. 5); each of said plurality of register files (RFs inside chips 51-54, see Fig. 5) is connected to a bus (55, see Fig. 5), and a value written to a global register in one of said plurality of register files is propagated (see Col. 4, lines 42-47, regarding the data written by any ALUs is "broadcast" via bus 55 to all registers) to a corresponding global register in

the other of said plurality of register files across said bus (55, see Fig. 5); and said plurality of register files (RFs inside chips 51-54, see Fig. 5) are connected together in serial, and a value written to a first global register in a first of said plurality of register files is propagated (see Col. 4, lines 42-47, regarding the data written by any ALUs is "broadcast" via bus 55 to all registers) to a corresponding first global in a second of said plurality of register files connected directly to said first of said plurality of register files (RFs inside chips 51-54, see Fig. 5).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Masubuchi'817's system to comprise the feature that when a value is written to one of said Q-number of said registers which is a global register within one of said plurality of register files, said value is propagated to a corresponding global register in the other of said plurality of register files; each of said plurality of register files is connected to a bus, and a value written to a global register in one of said plurality of register files is propagated to a corresponding global register in the other of said plurality of register files across said bus; and said plurality of register files are connected together in serial, and a value written to a first global register in a

first of said plurality of register files is propagated to a corresponding first global in a second of said plurality of register files connected directly to said first of said plurality of register files, as taught by Cook'340, in order to minimize the number of pins required and using very large scale integration technique, high densities can be achieved; and to eliminate off-chip delays, and performance is further enhanced by the shorter wire lengths in the registers for the Masubuchi'817's system (see Col. 2, lines 34-40).

As to claims 2 and 12, Masubuchi'817 discloses a VLIW computer comprising: every two of said N number of processing paths (for ALUs 13 and 14, se Fig. 1) share one (register file 12, see Fig. 1) of said plurality of register files (register files 12 and 22, see Fig. 1).

As to claims 3 and 13, Masubuchi'817 also discloses: a processing instruction comprises N-number of P-bit instructions appended together to form a very long instruction word (VLIW) (see col. 4, lines 6-12), and said N-number of processing paths process N number of P-bit instructions in parallel (note the above N, P, and M are variant. Masubuchi'817's VLIW is inherently having N, P, and M bit number).

As to claim 21, Masubuchi'817 also discloses: said Q-number of registers within each of said plurality of register files (12

and 22, see Fig. 1) can be switch between being either private or global(since they can be used as both private and global registers).

5. Claims 4 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masubuchi'817 in view of Cook'340 as applied to claims 1-3, 5-13, 15, 16, and 18-21 above, and further in view of Drabenstott et al. (U.S. Patent No. 6,366,999) hereafter referred to as Drabenstott et al.'999 and Ito et al. (U.S. Patent No. 6,615,339), hereafter referred to as Ito et al.'339.

Masubuchi'817/Cook'340 discloses the claimed invention except for explicitly showing: using M=64, Q=64, and P=32.

Drabenstott et al.'999 discloses a system comprising M=64 (see 64 bit data type in table 2), and P=32 (see 32 bit instruction bus 102 in Fig. 1).

Ito et al.'339 discloses a system comprising Q=64 registers (R0, R1, …, R63, see Fig. 4A) in the register file (40, see Fig. 4A).

Masubuchi'817/Cook'340's system will increase the speed of data movement and data management if a wider data and instruction size and more registers for register to register

data reference are used. Therefore, the performance will be enhanced.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Masubuchi'817/Cook'340's system to comprise M=64, Q=64, and P=32, as taught Drabenstott et al.'999 and Ito et al.'339, in order to increase the speed of data movement by using the bigger data size (64 bits) and using register to register data reference for the Masubuchi'817/Cook'340's system.

Further, as shown in re Rose, 105 USPQ 237 (CCPA 1955), to make changes in size/range generally does not provide patentable weight to the claimed invention.

Response to Amendment

6. Applicant's arguments mailed 1/11/05 have been considered but are moot in view of the new ground(s) of rejection. As set forth in the art rejections above, Masubuchi'817, Cook'340 and Ito et al.'339 teach the claimed invention.

Allowable Subject Matter

7. Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claim 18 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Greim et al.'628 discloses a DSP intercommunication network. The CPU 20 offers

only an address space of 4 MB (max) in its asynchronous window (CEO). Some resources, including private registers associated with the CPU 20, the local side of the CPU 20 DPSRAM 34, and the random access daughterboard interface need to be accessible at all times, this local address space is divided into two sections, a local section and a global section. This allows global accesses to exist in the lower 2 MB and private resources associated therewith to exist in the upper 2 MB.

Contact Information

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (571) 272-4162. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to **the TC central telephone number, 571-272-2100.**

11. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number: 703-872-9306.** This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER

March 7, 2005